IN THE SPECIFICATION

Please replace paragraph [0002], with the following rewritten paragraph:

[0002] The present invention relates to a surface computer and a computing method capable of rapidly performing various types of complex computations ~~at high speed~~, such as physical computations, environmental computations, behavior computations, ~~emotion~~ computations for emotional expressions and the like, by concurrently computing computation data contained in a two-dimensional region in units of two-dimensional regions.

Please replace paragraph [0024], with the following rewritten paragraph:

[0024] Fig. 12 is a block diagram showing another construction of the ~~important~~main part of the surface computer;

Please replace paragraph [0025], with the following rewritten paragraph:

[0025] Figs. 13A and 13B ~~is~~are ~~a~~ diagrams showing ~~an~~ instruction words;

Please replace paragraph [0039], with the following rewritten paragraph:

[0039] The concept of "surface region data" (that is, data represented by any geometric (2D, 3D, etc.) surface for any type of data which can be depicted or represented as a geometric surface) means a set of computation data which exists in a surface region. Accordingly, the concept of a "surface computer" is a computer that specifies surface region data based on a surface or a surface region, manipulates it (i.e., reads data from memory and writes data to it) and performs computing processing. Since the surface computer processes surface region data, which is a group of data having a certain large quantity, processed data itself has the concept of concurrence or parallelism. That is, the data has a structure capable of being ~~concurrently~~ processed in parallel.

Please replace paragraph [0051], with the following rewritten paragraph:

[0051] The PP 9 computes the surface region corresponding to an operand of a surface computing instruction word and issues an instruction that computation data corresponding to this surface region is transferred from the DRAM 1 to primary and secondary ~~sense amplifiers~~buffers 10 and 11 ~~(buffers)~~ which are included in the DRAM 1. ~~The primary~~ Alternatively, a sense-amplifier ~~10 and the secondary sense-amplifier 11 serve as~~or a cache memory can be used as a substitute for the buffers. As such, the primary buffer 10 and the secondary buffer 11 are also referred to herein as the primary sense-amplifier 10 and the secondary sense-amplifier 11. Furthermore, the PP 9 sets up the AG 3 in accordance with the operand. In addition, the PP 9 decodes general-purpose surface computing instructions which are called from the main memory 7 and which are fetched via the IFU 2.

Please replace paragraph [0052], with the following rewritten paragraph:

[0052] The AG 3 generates an address for providing data fetched in the sense-amplifiers 10 and 11 to the PA 4, computes location dependence information within the surface regions, and outputs the resultant location dependence information to the PA

4. Computation of location dependence information means, for example, ~~address~~ computation of an address for adjusting surface region data when the surface region sizes which determine the corresponding surface region data (objects to be computed) disagree and when an address of one surface region having data thereat corresponds to the address of the other surface region having no data thereat. Enlarging/reducing processing, interpolation processing such as bilinear interpolation processing or tri-linear interpolation processing, and the like for computation of location dependence information are described below.